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(54) Hidden-surface processing device, anti-aliasing method and three-dimensional graphics processing apparatus.

(57) The present invention intends to provide a three-dimensional graphics processing apparatus which can execute hidden-surface processing, smooth shading processing and anti-aliasing processing. The conventional hidden-surface processing device can only provide pixel information such as luminance data, and so cannot execute any processing requiring error data at polygon boundaries, such as anti-aliasing processing. The conventional anti-aliasing method must deal with many cases because the processing is made for each pixel, execute complicated calculation if the boundary line extends over several pixels, and may not able to process the display with decimals omitted. The hidden-surface processing device according to the present invention is provided with an error register (15) which can hold error data at polygon boundaries and its output means thereby to provide the error data at the polygon boundaries. The anti-aliasing method according to the present invention can replace the information on two successive pixels at polygon boundaries by its area average on two successive pixels on one scan line and output the replaced information, which is very efficient for real-time processing.

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HIDDEN-SURFACE PROCESSING DEVICE, ANTI-ALIASING METHOD AND THREE-DIMENSIONAL GRAPHICS PROCESSING APPARATUS

BACKGROUND OF THE INVENTION

The present invention relates to a graphic processing device and method in a field of computer graphics.

When a three-dimensional object is projected on a two-dimensional screen, an object partially or entirely shades other objects behind it. In order to obviate such an undesired phenomenon, a scan-line algorithm has been proposed which executes sequential processings using a general-purpose processor. A Z-buffer algorithm has been also proposed which is suitable to be implemented in hardware. The scan-line algorithm, when luminance data of each of pixels are displayed for each raster scan as in CRT, uses a very strong correlation between a pixel and adjacent pixels or a pixel on a subsequent scan line. Although this algorithm is suitable to execute sequential processings, it has a disadvantage of requiring a large number of calculations and complicating control logic. On the other hand, the Z-buffer algorithm previously stores for each of pixels the color and luminance (represented by the luminance) of a plane displayed on each pixel and the depth of the plane, and compares the depth of a new plane with the stored depth whenever the new plane is input; then only when the depth of the new plane is smaller than the stored depth, the stored depth is updated and also the luminance of the new plane is registered. Therefore, although the Z-buffer algorithm requires depth registers (generally, called 'Z-buffers') to be provided for all the pixels and so a very large memory circuit, it has an advantage of comparatively simple control logic.

As an intermediate method of those hidden-surfaces elimination algorithms, a method using a correlation between scan lines and the Z-buffer algorithm within one scan line is disclosed in N. Gharachorloo and C. Pottole, "Super buffer: A systolic VLSI graphics engine for real time raster image generation", 1985 Chapel Hill Conference on Very Large Scale Integration, pp. 285 - 305. The hardware to implement this method, however, is too large so that it is difficult to realize the entire array in LSI.

The inventors of the present invention proposed a hidden-surface processing device disclosed in JP-A-62-100878 which is suitable to be realized in LSI with less hardware.

Fig. 8 is a system block diagram of the proposed hidden-surface processing device. Fig. 9 is a view showing the details of each of pixel processors which constitute the hidden-surface processing device. In Figs. 8 and 9, 1 is a pixel processor corresponding to each of N pixels on one scan line; 10 is a depth register for registering the depth coordinate of a plane nearest to the screen in terms of pixel positions; 11 is a luminance register for registering the luminance information of the plane; and 12 is an adder for deciding whether or not the pixel processor is within a range where a plane segment is located, adding displacement in the depth, comparing depth data and adding a displacement in luminance data in a time division manner.

Referring to a conceptual view of Fig. 10, explanation will be made on the operation of the hidden-surface processing device thus constructed.

A plane 200 is defined in a three-dimensional space (generally called a normalized device coordinate system) as shown in Fig. 10 in which a depth coordinate, a z-coordinate is added to the x-y coordinate system corresponding to an M x N two-dimensional screen. The plane 200 is projected on the x-y plane to be displayed on the screen. With the raster-scan CRT, this processing is performed for each horizontal scan line so that it will be performed on the section 201 provided by cutting the plane 200 with a plane (generally called a scan line plane) passing the present scan line and in parallel to the x-z plane. This section 201 is called a plane segment. The individual plane segment has elements of a left end point coordinate (XL, ZL), the number of successive pixels (dX), a z-coordinate displacement for each pixel (Z'), luminance information I at the left end point, and a luminance displacement I' for each pixel. The token having these items of information is input in a manner divided into an A input port Ai and a B input port Bi to a left end pixel processor 1 of the pixel processors formed in an array as shown in Fig. 8. Control information CTRLi includes IN flag information indicative of that the corresponding pixel processor is within a range where the plane segment in question is located. The information given to the respective ports in a time divisional manner are tabulated as shown in Fig. 11.

The operation of each pixel processor is as follows.

At a first timing T1, data at the A input port Ai and an all 1 pattern are supplied to an adder 12 to provide the subtraction result of the A input data minus 1. If the IN flag = 0, and the subtraction result is negative, it means that the pixel processor has entered the range where the plane segment is located. Then, the data dX at the B input port Bi is shifted to the A port by the selector 14 to enter the

latch 17. Also the IN flag is inverted to 1 to enter the latch 16. If the IN flag = 1, and the subtraction result is negative, it means that the pixel processor has gone out from range where the plane is located. Then, the IN flag is inverted to 0 to output the negative value (the maximum value in integers with no sign) to the A output port as it is. In other cases, the CTRLi is output to CTRLo as it is and the addition result is output to the A output port Ao.

At a second timing T2, if the IN flag = 1, Z at the A input port Ai and Z′ at the B input port Bi are added to produce the addition result at the A output port Ao. If the IN flag = 0, Z at Ai is output to Ao as it is without being updated.

At a third timing T3, Z at Ao at the timing T2 is held as it is. Then, with the IN flag = 1, Z at Ai and Zb in the depth register 10 are compared by the adder 12. If the comparison result is Z < Zb, Z at Ai will be stored in the depth register 10.

At a fourth timing T4, if the IN flag = 1 and the above comparison result is Z < Zb, I at the B input port Bi will be stored in the luminance register 11, and I at Ai and I; at Bi are added to produce the addition result at Ao. In other cases, I at Ai is output to Ao as it is without being updated.

At the above four all timings, the value at Bi is output at Bo as it is through the latch 18.

Fig. 12A shows the state where the token as described above flows along the array of pixel processors while being subjected to the processing by each pixel processor. Upon completion of processing all the tokens on one scan line, the luminance data of the segment nearest to the corresponding pixel positions is stored in the luminance register in each pixel processor.

The operation of each pixel processor for a sweep token will be explained which reads the contents of the luminance register of each pixel processor and initializes the contents of a depth register and the luminance register. As understood from the above description, it is possible to insert, in the timing slot of T2 or T3 unused on the bus of the CTRL signal, a discriminator for discriminating whether the token is a plane segment or a sweep token. At the first timing T1, the number DPR of displayed pixels on one scan line is received in place of X, and 1 is subtracted from it to count the remaining number of displayed pixels. Then, that the subtraction result is negative means that the token has deviated from the display range so that the IN flag is inverted to 0. At the second timing T2, if the token is within the display range with IN flag = 1, the pixel processor 1 sends the data in the luminance register 11 to the luminance data bus. At the third timing T3, if the token is within the display range with IN flag = 1, an initial value Z back is stored in the depth register 10. At the fourth timing T4, if the token is within the display range with IN flag = 1, an initial value I back is stored in the luminance register 11.

Fig. 12B shows the state where the sweep token as described above flows along the array of pixel processors while being subjected to the processing by each pixel processor. In this way, the luminance data of the segment nearest to the pixels on one scan line are successively read out from each pixel processor.

Meanwhile, the conventional anti-aliasing algorithm along a scan line is disclosed in e.g. 'COMPUTER GRAPHICS' by E. Nakamae, edited by DENSITSUSIN GAKKAI, 1987, PP. 183 - 186.

This anti-aliasing algorithm will be explained below.

If the x coordinate of a boundary of a plane segment has a minimum value XMIN and a maximum value XMAX within the same pixel as shown in Fig. 13A, the shaded portion is a trapezoid. Then, the luminance of the pixel is corrected by the rule X0 · IL + (1-X0) · IR, assuming that the luminance in the shaded portion of the pixel is IR and that in the remaining left portion is IL, and the width X0 of the remaining portion on the X central line is X0 of the pixel. Further, if the boundary of the plane segment extends over some pixels as shown in Fig. 13B, the luminance of each of the intermediate pixels is corrected by the rule of Yn · 1L + (1 - Yn) · IR (n = 0, 1, 2, ...) assuming that the width of the remaining portion on the Y central line of each of the intermediate pixels is Y0, Y1, Y2 ... Yn; this is also because the shaded portions in the intermediate pixels other than the pixels at both ends are trapezoids. The luminance of the first and the last pixel can be corrected on the basis of that they include a triangle and a pentagon (a triangle or trapenzoid as the case may be). Otherwise, it can be defined as IL or IR admitting some error.

The hidden-surface processing device having the constructions as mentioned above has a disadvantage that the processing using error data such as anti-aliasing cannot be performed using only the data directly obtained from the device.

The above anti-aliasing method requires decision relative to XMIN and XMAX, and also requires to calculate Y0, Y1 and Y2 if the boundary of the plane segment extends over plural pixels as shown in Fig. 13B; this calculation is time-consuming and so is difficult to carry out in real time. Further, if the data corresponding to one scan line are successively output, it is necessary to once store the data somewhere for the anti-aliasing processing. Further, the graphic display device in which the luminance is omitted in its decimals generates the state as shown in Fig. 14. Specifically, up to the pixel A is painted for boundary 1 while up to the pixel B is painted for boundary 2. In this case, if the aliasing is removed by the above

conventional anti-aliasing method, the luminance of the pixel A can be corrected at the boundary 1 and that of the pixel C can be corrected for the boundary 2. The corrected color for the pixel B, however, cannot be decided unless the color before drawing the boundary 2 is held.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a hidden-surface processing device which can directly produce luminance data and error data and so can be used to execute the processing requiring the error data such as anti-aliasing processing.

Another object of the present invention is to provide an anti-aliasing method which can continuously execute an anti-aliasing processing using the luminance data corresponding to one scan line and the error data of the plane to be displayed at its boundary which are successively obtained and so is suitable to real-time processing, and can correct the pixel state which can occur as shown in Fig. 14 in a graphic display device in which the luminance is omitted in its decimals for display.

Still another object of the present invention is to provide a three-dimensional graphics processing device which can execute in real-time a hidden-surface processing, smooth shading and anti-aliasing processing.

In accordance with one aspect of the present invention, there is provided a hidden-surface processing device comprising a depth register for holding the depth of a plane segment nearest to each of pixels on the basis of an input of plane segment information on one scan line of the screen; a luminance data register for registering luminance data; an error register for registering errors of the plane segment at its boundary and their related error information; an adder for deciding whether or not the pixel processor is within a range where a plane segment is located, adding displacement in the depth, comparing depth data and adding a displacement in luminance data in a time division manner; input/output means for updating information on an input plane segment token and outputting the updated information through one stage pipeline register; a luminance data bus for externally outputting the contents of the luminance register; and a error data bus for externally outputting the contents of the error register.

In accordance with another aspect of the present invention, there is provided an anti-aliasing method comprising the steps of error decision of, on the basis of errors of the coordinate values of two successive pixels on one scan line and error information deciding if the errors are due to a left boundary, a right boundary or the part other than the boundaries, deciding a combination of said items of error information and selecting errors of said two pixels; correction calculation of, on the basis of an input of said errors and pixel information of said two pixels, calculating an average (proportional distribution) of said pixel information between said two pixels in their area using said decision result; and replacement output of, on the basis of the said decision result, said correction calculation result and said pixel information, outputting said pixel information of said two pixels after it has been decided whether or not they should be replaced by the correction calculation result.

In accordance with still another aspect of the present invention, there is provided a three-dimensional graphics processing apparatus comprising a hidden-surface processing device; an error decision device for deciding, on the basis of inputs of errors En, En+1, and items of error information Fn, Fn+1, a combination of the items of error information Fn, Fn+1 thereby to select En if the combination is that of a right boundary and the part other than boundaries or that of a right boundary and a right boundary, En+1 if the combination is that of the part other than boundaries and a left boundary, or that of a left boundary and a left boundary, and a larger one of En and En+1 if the combination is that of a right boundary and left boundary; a correction calculation device for calculating, on the basis of inputs of the error En or En+1 selected by the error decision device and luminance data In, In+1, $I = \{(In + In+1) + Ex\ (In - In+1)\}/2$ (where x = n or n+1); and a replacement output device, on the basis of inputs of the decision by the error decision device, the calculation result I by the correction calculation device and the luminance data In, In+1, for outputting the luminance data In replaced by the calculation result I by the correction calculation device if the combination of Fn and En+1 is that of a right boundary and the part other than boundaries, or that of a right boundary and a right boundary, the luminance data In+1 replaced by I if the combination is that of the part other than boundaries and a left boundary, or that of a left boundary and a left boundary, both luminance data In and In+1 replaced by I if the combination is that of a right boundary and a left boundary, and outputting the luminance data In and In+1 without being replaced by I in other cases, where among luminance data, error data and their information representing if the error is due to a left boundary, a right boundary or that other than the boundaries corresponding to one scan line outputted from the hidden-surface processing device, the In and In+1 (n: integer ≧ 0) are two successive pixels, En and En+1 are errors in the coordinates of the respective pixels, and Fn and Fn+1 are their error related information.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a hidden-surface processing device according to the first embodiment of the present invention;

Fig. 2 is a block diagram of an array of pixel processors according to the first embodiment;

Figs. 3A and 3B are tables for explaining classification of error information and input tokens, respectively, in the first embodiment;

Figs. 4A and 4B are views showing the state where tokens flow through pixel processors in the first embodiment;

Fig. 5 is a schematic block diagram of an arrangement of the second embodiment of the present invention;

Figs. 6A and 6B are views for explaining correction calculation in the second embodiment of the present invention;

Fig. 7 is a system block diagram of three-dimensional graphics processing apparatus according to the third embodiment of the present invention;

Fig. 8 is a block diagram of the prior art hidden-surface processing device;

Fig. 9 is a block diagram of the pixel processor in the prior art hidden-surface processing device;

Fig. 10 is a view for explaining the concepts common to the present invention and the prior art;

Fig. 11 is a table for explaining an input token in the prior art hidden-surface processing device;

Figs. 12A and 12B are views showing the state where tokens flow through pixel processors in the prior art hidden-surface processing device;

Figs. 13A and 13B are views for explaining the prior art anti-aliasing method; and

Fig. 14 is a view for explaining the case which cannot be processed by the prior art anti-aliasing method.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a system block diagram of the hidden-surface processing device according to the first embodiment of the present invention.

Fig. 2 is a view showing the details of each of pixel processors which constitute the hidden-surface processing device. In Figs. 1 and 2, 1 is a pixel processor corresponding to each of N pixels on one scan line; 10 is a depth register for registering the depth coordinate of a plane nearest to pixel positions; 11 is a luminance register for registering the luminance information of the plane; and 12 is an adder for deciding whether or not the pixel processor is within a range where a plane segment is located, adding displacement in the depth, comparing depth data and adding a displacement in luminance data in a time division manner; 15 is an error register for registering an error of the plane at its boundary and error information representing whether the error is due to the left boundary of the plane or the right boundary thereof.

Explanation will be given for the operation of the hidden-surface processing device according to this embodiment.

Now it is assumed that a token has as information of a plane segment, elements of a left end point coordinate (XL, ZL), the number of successive pixels (dX), a z-coordinate displacement for each pixel (Z'), luminance information I at the left end point, and a luminance displacement I' for each pixel, an error EL at the left end point (left boundary), and an error ER at the right end point (left boundary). The token having these items of information is input in a manner divided into an A input port Ai and a B input port Bi to a left end pixel processor 1 of the pixel processors formed in an array as shown in Fig. 1. It should be noted that error information is included in high order two bits of the error EL at the left end point and of the error ER at the right end point. The error information can be tabulated as shown in Fig. 3a. Control information CTRLi includes IN flag information indicative of that the corresponding pixel processor 1 is within a range where the plane segment in question is located. The information given to the respective ports in a time divisional manner are tabulated as shown in Fig. 3B.

The operation of the pixel processor will be explained with reference to Fig. 2.

At a first timing T1, data at the A input port Ai and an all 1 pattern are supplied to an adder 12 to provide the subtraction result of the A input data minus 1. If the IN flag = 0, and the subtraction result is negative, it means that the pixel processor has entered the range where the plane segment is located. Then, the data dX at the B input port Bi is shifted to the A port by the selector 14 to enter the latch 17. Also the IN flag is inverted to 1 to enter the latch 16. If the IN flag = 1, and the subtraction result is negative, it means that the pixel processor has gone out from range where the plane is located. Then, the IN flag is inverted to 0 to output the negative value (the maximum value in integers with no sign) to the A output port as it is. In other cases, the CTRLi is output to CTRLo as it is and the addition result is output to the A output port Ao.

At a second timing T2, if the IN flag = 1, Z at the A input port Ai and Z' at the B input port Bi are added to produce the addition result at the A output port Ao. If the IN flag = 0, Z at Ai is output to Ao as it is without being updated.

At a third timing T3, Z at Ao at the timing T2 is

held as it is. Then, with the IN flag = 1, Z at Ai and Zb in the depth register 10 are compared by the adder 12. If the comparison result is Z < Zb, Z at Ai will be stored in the depth register 10.

At a fourth timing T4, if the IN flag = 0 and the above comparison result is Z < Zb, I at the B input port Bi will be stored in the luminance register 11, and I at Ai and I′ at Bi are added to produce the addition result at Ao. In other cases, I at Ai is output to Ao as it is without being updated.

Finally, at a fifth timing T5, when the IN flag is inverted from 0 to 1, i.e. when at the first timing T1, IN flag = 0 and the subtraction result of X is negative, and also if the comparison result at the third timing T3 is Z < Zb, EL on the A input port is stored in the error register 15 to update the contents thereof. Also when the IN flag is inverted from 1 to 0, i.e. when the IN flag = 1 and the subtraction result of dX is negative, and also the comparison result at the third timing T3 is Z < Zb, ER on the B input port is stored in the error register 15 thereby to update the contents thereof. In other cases, EL at Ai and ER at Bi are outputted to the A output port Ao and the B output port Bo as they are.

Fig. 4A shows the state where the token having the plane segment information as described above flows along the array of pixel processors while being subjected to the processing by each pixel processor.

As understood from the above description, it is possible to insert, in the timing slot of T2 or T3 unused on the bus of the CTRL signal, a discriminator for discriminating whether the token is a plane segment or a sweep token.

Referring to Fig. 2 and Fig. 4B, explanation will be made on the operation of each pixel processor when it receives the sweep token.

At the first timing T1, the number of displayed pixels on one scan line is received in place of X, and 1 is subtracted from it to count the remaining number of displayed pixels. Then, that the subtraction result is negative means that the sweep token has deviated from the display range so that the IN flag is inverted to 0.

At the second timing T2, if the sweep token is within the display range with IN flag = 1, the pixel processor 1 sends the contents in the luminance register 11 to the luminance data bus IBUS and those of the error register 15 to the error data bus EBUS.

At the third timing T3, if the sweep token is within the display range with IN flag = 1, an initial value Z Back is stored in the depth register 10.

At the fourth timing T4, if the sweep token is within the display range with IN flag = 1, an initial value I Back is stored in the luminance register 11.

At the fourth timing T5, the sweep token is within the display range with IN flag = 1, all the bits in the error register 15 are initialized to 0.

In this way, the sweep token moves to the adjacent pixel processor for each timing, so that the luminance to be displayed for each pixel and the error at the boundary are successively output from the luminance data bus and the error data bus. Therefore, if the above process is carried out fro scan lines corresponding to one image plane, and this is repeated, the luminance data and the errors at the boundary of a plane to be displayed can be simultaneously obtained. Thus, the processing requiring to use errors such as anti-aliasing can be executed at a very high speed.

Now referring to Figs. 5 and 6, explanation will be given for the anti-aliasing method according to the second embodiment of the present invention. Fig. 5 is a block diagram for explaining the process of the anti-aliasing method according to this embodiment. Fig. 6 is a view for explaining the correction calculation used in the anti-aliasing method according to this embodiment.

It is assumed that the luminance data for two successive pixels on one scan line are In and In+1 (n: integer ≥ 0) and the errors of the coordinate values for these pixels are En and En+1. The error of the coordinate value is a distance from the center of a pixel on which a boundary is displayed to the boundary along the center line of a scan line (see Fig. 6). It should be noted that if the decimals thereof are rounded off for display, the distance takes a plus or minus sign. Specifically, the sign is plus or minus according as the boundary is located on the right or left side of the pixel center. If the decimals of the distance are omitted for display, the sign may be only plus. The information deciding if the error is due to a left boundary, a right boundary or the part other the boundaries is referred to as error information. It is assumed that the respective items of information corresponding to the above two pixels are Fn and Fn+1. In this case, the combinations of Fn and Fn+1 are classified as follows.

(1) Fn: other than boundaries, Fn+1: left boundary

(2) Fn: left boundary, Fn+1: left boundary

(3) Fn: right boundary, Fn+1: other than boundaries

(4) Fn: right boundary, Fn+1: right boundary

(5) Fn: right boundary, Fn+1: left boundary

(6) combination other than the above combinations

Error decision means 20 decides the combination on the basis of inputs of the errors En and En+1, and the error information Fn and Fn+1 according to the above classification. If the decision result is (1) or (2), En+1 is selected. If it is (3) or (4), En is selected. If it is (5), a not smaller one of

En and En+1 is selected. If it is (6), either may be selected. The selected error is sent to correction calculation means 21. The correction calculation means 21 performs, on the basis of inputs of the error Ex (x = n or n+1) output from the error decision means 20 and the luminance data In, In+1 as described above, the following calculation (-)

$$I = \{(In + In+1) + Ex \cdot (In - In+1)\} /2 \ldots (-)$$

where x = n or n+1

Equation (-) will be explained with referring to Figs. 6A and 6B. Fig. 6A show the case of the above class (3). In this case, the n-th and (n+1) pixels are parallel-shifted to left by 1/2 of the pixel width (so as to form a square indicated by a dotted line). Using the area ratio of the parallel-shifted pixels, the luminance is determined like Equation (-).

Fig. 6B show the case of the above class (1). In this case, the n-th and (n+1) pixels are parallel-shifted to right by 1/2 of the pixel width (so as to form a square indicated by a dotted line). Using the area ratio of the parallel-shifted pixels, the luminance is determined like Equation (-). Likewise, with respect to the classes (2) and (4), the luminance can be determined. On the other hand, in the case of the class (5), the luminance is determined using the larger error. Incidentally, the above equation is approximate in accordance with the gradient of the boundary line.

The result I of Equation (-) calculated by the correction output means 22 is sent to replacement output means 22. The replacement calculation means 21, on the basis of inputs of the calculation result of Equation (-), and In and In+1, replaces In+1 by I if the class decided by the error decision means 20 is (1) or (2), In by I if the class is (3) or (4), both In and In+1 by I if the class is (5), and outputs them as they are without being replaced it the class is (6).

In this way, the correction calculation for anti-aliasing is made using successive two pixels and the calculation result is replaced by original data to provide the data after the anti-aliasing. Therefore, successive data are successively processed so that anti-aliasing can be performed for the case as shown in Fig. 14.

Finally, explanation will be given for the three-dimensional graphics processing apparatus according to the third embodiment of the present invention. Fig. 7 is a system block diagram of the three-dimensional graphics processing apparatus according to this embodiment. In Fig. 7, 30 is the hidden-surface processing device according to the first embodiment. The operation of the three-dimensional graphics processing apparatus will be explained in connection with Fig. 7.

First, plane segment information corresponding to one scan line are input in a manner divided into an A input port Ai and a B input port Bi on the left side of the hidden-surface processing device according to the first embodiment. As previously described, it should be noted that the plane segment information is tokens each having elements of a left end point coordinate (XL, ZL), the number of successive pixels (dX), a z-coordinate displacement for each pixel (Z'), luminance information I at the left end point, and a luminance displacement I' for each pixel, an error EL at the left end point (left boundary), and an error ER at the right end point (right boundary). Further, it should be also noted that high order bits of the error EL at the left terminal point and the error ER at the right terminal point include the error information as tabulated in Fig. 3A.

When sweep tokens are input subsequently to the plane segment tokens, luminance data and boundary error data corresponding to one scan line are successively output from the luminance data bus (IBUS) and the error data bus (EBUS) of the hidden-surface processing device 30, respectively. It is assumed that the luminance data successively output from the luminance data bus (IBUS) are I0, I1, I2, ..., the error data successively output the error data bus (EBUS) are E0, E1, E2, ..., and items of the error information are F0, F1, F2, ... The luminance data In and In+1 of successive two pixels from the luminance data bus (IBUS) are stored in an I register B 42 and an I register A 41. During this period, En, En+1 and Fn, Fn+1 from the error data bus (EBUS) are stored in an E register B 32, an E register A 31, an F register B 34 and an F register A 33, respectively. The contents of error information stored in the F register B 34 and the F register A 33 are decided by an error information decision device 35 as follows.

(1) when Fn = 00, Fn+1 = 10,
(2) when Fn = 10, Fn+1 = 10,
(3) when Fn = 01, Fn+1 = 00,
(4) when Fn = 01, Fn+1 = 01,
(5) when Fn = 01, Fn+1 = 10,
(6) other cases

The error information decision device 35 sends the decision result to a selector A 36. The selector A 36 selects the contents of the E register A 31 or the E register B 32. Specifically, if the decision result is (1) or (2), En+1 from the E register A 31 is selected; if it is (3) or (4), En from the E register B 32 is selected; if it is (5), a larger one of En and En+1 is selected; and if it is (6), either may be selected. The selected En or En+1 will be sent to an E register C37. On the other hand, the decision result by the error information decision device 35 is also sent to a K register A 37. During these processings, the contents of both I register B 42 and I register B 41 are sent to a subtractor 43 and an

adder A 44, and also successively sent to an I register E 47. The subtractor 43 calculates In - In+1 to send the result to an I register C 45. The adder A 44 calculates In + In+1 to send the result to an I register D 46. The contents of the I register C 45 and ET (T = n or n+1) selected by the selector A 36 which is the contents of the I register C 37 are multiplied together by a multiplier 48 thereby send the result of (In - In+1) · ET (T = n or n+1) to an I register F 49. During this processing, the contents of the K register A 38 are sent to a K register B 39; those of the I register D 46 are sent to an I register G 50; and those of the I register E 47 are sent to an I register H 51. The contents of both the I register F 49 and the I register G 50 are sent to an adder B 52 with a one-bit right shifter which calculates {(In + In+1) + (In - In+1) · ET}/2 (T = n or n+1); this result will be sent to an I register I 53. During this addition processing, the contents of the K register B 39 are a K register C 40 and those of the I register H 51 are sent to an I register J 54. Next, the decision result by the error decision device 35, which is the contents of the K register C 40, is sent to a selector B 56. The selector B 56 stores two decision results with a priority of the decision result early stored, and selects I, In or In+1 in the following manner.

If the decision result sent from the K register C 40 is (1) or (2), the contents In of the I register J 54 are selected to be sent to a display device. At the next timing, I which has been from the I register I 53 to the I register K 55 is selected in place of In+1 to be sent to the display device. If it is (3) or (4), I which is the contents of the I register I 53 is selected in place of In which is the contents of the I register J 54 so as to be sent to the display device. If it is (5), I which is the contents of the I register I 53 is selected in place of In which is the contents of the I register J 54 so as to be sent to the display device. At the next timing also, the I, which has been sent from the I register I 53 to the I register K 55, is selected in place of In+1 so as to be sent to the display device. If it is (6), the contents of the I register J 54 are successively selected to be sent to the display device. In short, if the decision result is (1) or (2), I is outputted in place of In+1; if it is (3) or (4), I is outputted in place of In; if it is (5), I is outputted in place of both In and In+1; and if it is (6), In and In+1 are outputted as they are.

If the above process is executed for scan lines corresponding to one image plane and it is further repeated, a three-dimensional polyhedral object, while being subjected to a hidden-surface processing, a smooth shading processing and anti-aliasing processing, can be displayed on a two-dimensional display screen in real time.

As understood from the above description, the hidden-surface processing device according to the present invention comprises an error register which can store errors of a plane segment on one scan line nearest to pixels at its boundaries, and error information indicative of whether the error is due to a left boundary or a right boundary, and an error data bus which can read the storage contents together with the luminance data.

Further, the anti-aliasing method according to the present invention executes correction for boundaries on the pixels using two successive pixels on one scan line so that it is not necessary to decide whether the boundary is located within one pixel or extended over plural pixels and it is possible to obviate troublesomeness in correction calculation where the boundary is extended over plural pixels. The correction can be made for the case as shown in Fig. 14 in a graphic processing apparatus providing a display with decimals omitted. Further, it is possible to successively process one-scan-line data successively produced.

In accordance with the present invention, when plane segment information on one scan line supplied to a hidden-surface processing device is processed to provide luminance data and error data in real time so that anti-aliasing processing can be continuously executed using these data successively produced. Thus, the hidden surface processing, smooth shading processing and the anti-aliasing processing can be carried out in real time.

In accordance with the hidden-surface processing device of the present invention, the luminance of a plane to be displayed at a high speed and errors at its boundaries are obtained which can be used for anti-aliasing processing. Further, an accordance with the anti-aliasing method of the present invention, even when the luminance data and the error data corresponding to one scan line are successively produced, the anti-aliasing can be executed without being stored somewhere, and so in real time. Further, in accordance with the three-dimensional graphics apparatus of the present invention, a three-dimensional polyhedral object, while being subjected to hidden-surface processing, smooth shading and anti-aliasing, can be displayed in a real time on a two-dimensional display screen. In this way, the present invention can provide very great industrial effects.

Claims

1. In a graphic display device for displaying a three-dimensional polyhedral object being subjected to hidden-surface processing on a two-dimensional screen, a hidden-surface processing device constituted by an array consisting of pixel processors (1) corresponding to pixels on one scan line

on a screen, each comprising:
a depth register (10) for storing the depth (Zb) of a plane nearest to the pixels;
a luminance register (10) for holding the luminance data (Ib) of the plane;
an error register (15) for holding errors at its boundaries and symbols deciding if the error is due to a left boundary, a right boundary, or the part other than the boundaries;
an adder (12);
means for inputting, from the pixel processor corresponding to an adjacent previous stage pixel, a token having segment information on a plane segment obtained when a polygon is cut by a scan line plane, said segment information including elements of a head pixel position (X), the number (dX) of successive pixels, the depth (Z) corresponding to the head pixel, a depth displacement (dZ/dX) for each pixel unit, the luminance data (I) corresponding to the head pixel, the error data (EL) corresponding to the head pixel, and the error data (ER) corresponding to an end pixel;
means for outputting the token having the updated segment information to the pixel processor corresponding to an adjacent subsequent pixel through one-stage pipe line register;
means for externally reading the luminance data (Ib) in said luminance register; and
means for externally reading the error data in said error register;
wherein in the case where the plane segment information is input to said pixel processor, whether the pixel processor in question is included in the range where a new plane segment on the scan line in question is located is decided in the basis of the head pixel position (X) or the number (dX) of successive pixels input to said adder (12) by said inputting means, and if the pixel processor is within the range, the displacement data (dZ/dX) is added to the depth data (Z) by said adder to send its result to a subsequent pixel processor; the depth data (Z) is compared with the depth data in question in said depth register (10) by said adder (12) to decide whether Z < Zb (or Z ≤ Zb), and only if the decision result is yes, the contents of said depth register (10) and said luminance register (11) are replaced by the depth data (Z) and the luminance data (I) of the new plane segment; and whether the pixel processor in question is a head or end in the range on the scan line where the new plane segment is located is decided on the basis of the head pixel position (X) or the number (dX) of successive pixels input to said adder (12), and only if the decision result is yes and also Z < Zb (or Z ≤ Zb), the contents of said error register are replaced by the error data (EL) corresponding to the head pixel of the new plane segment and a symbol indicative of the head pixel or the error data (ER) corresponding to the end pixel and a symbol indicative of the end pixel according as the pixel processor in question is at a head or end in the range on the scan line where the new plane segment is located; and
wherein in the case where a sweep token indicative of the end of one scan line is input to a previous pixel processor in place of the token having the segment information, after the data (Ib) stored in said luminance register (11) and the data (EL) or (ER) in said error register (15) are externally output, the contents of said depth register (10) are initialized to a maximum value, those of said luminance register (11) are initialized to background color, and those of said error register (15) are initialized to an initial state, and said sweep token is outputted to a subsequent pixel processor.

2. In a graphic display device for displaying a three-dimensional polyhedral object being subjected to hidden-surface processing on a two-dimensional screen, a hidden-surface processing device constituted by an array consisting of pixel processors (1) corresponding to pixels on one scan line on a screen, each comprising:
a depth register (10) for storing the depth (Zb) of a plane nearest to the pixels;
a luminance register (10) for holding the luminance data (Ib) of the plane;
an error register (15) for holding errors at its boundaries and symbols deciding if the error is due to a left boundary, a right boundary, or the part other than the boundaries;
an adder (12);
means for inputting, from the pixel processor corresponding to an adjacent previous stage pixel, a token having segment information on a plane segment obtained when a polygon is cut by a scan line plane, said segment information including elements of a head pixel position (X), the number (dX) of successive pixels, the depth (Z) corresponding to the head pixel, a depth displacement (dZ/dX) for each pixel unit, the luminance data (I) corresponding to the head pixel, the luminance displacement (dI/dX) for each pixel unit, error data (EL) corresponding to the head pixel, and the error data (ER) corresponding to an end pixel;
means for outputting the token having the updated segment information to the pixel processor corresponding to an adjacent subsequent pixel through one-stage pipe line register;
means for externally reading the luminance data (Ib) in said luminance register; and
means for externally reading the error data in said error register;
wherein in the case where the plane segment information is input to said pixel processor, whether the pixel processor in question is included in the range where a new plane segment on the scan line

in question is located is decided in the basis of the head pixel position (X) or the number (dX) of successive pixels input to said adder (12) by said inputting means, and if the pixel processor is within the range, the displacement data (dZ/dX) is added to the depth data (Z) by said adder to send its result to a subsequent pixel processor; the depth data (Z) is compared with the depth data in question in said depth register (10) by said adder (12) to decide whether Z < Zb (or Z ≤ Zb), the change data (dI/dX) is added to the luminance data (I) by said adder (12) to send the result to a subsequent pixel processor, and only if the above decision result is yes, the contents of said depth register (10) and said luminance register (11) are replaced by the depth data (Z) and the luminance data (I) of the new plane segment; and whether the pixel processor in question is a head or end in the range on the scan line where the new plane segment is located is decided on the basis of the head pixel position (X) or the number (dX) of successive pixels input to said adder (12), and only if the decision result is yes and also Z < Zb (or Z ≤ Zb), the contents of said error register are replaced by the error data (EL) corresponding to the head pixel of the new plane segment and a symbol indicative of the head pixel or the the error data (ER) corresponding to the end pixel and a symbol indicative of the end pixel according as the pixel processor in question is at a head or end in the range on the scan line where the new plane segment is located; and

wherein in the case where a sweep token indicative of the end of one scan line is input to a previous pixel processor in place of the token having the segment information, after the data (Ib) stored in said luminance register (11) and the data (EL) or (ER) in said error register (15) are externally output, the contents of said depth register (10) are initialized to a maximum value, those of said luminance register (11) are initialized to background color, and those of said error register (15) are initialized to an initial state, and said sweep token is outputted to a subsequent pixel processor.

3. In a graphic display device for displaying a three-dimensional polyhedral object being subjected to hidden-surface processing on a two-dimensional screen, a hidden-surface processing device constituted by an array consisting of pixel processors (1) corresponding to pixels on one scan line on a screen, each comprising:

a depth register (10) for storing the depth (Zb) of a plane nearest to the pixels;

a luminance register (10) for holding the luminance data (Ib) of the plane;

an error register (15) for holding errors at its boundaries and symbols deciding if the error is due to a left boundary, a right boundary, or the part other than the boundaries;

an adder (12);

means for inputting, from the pixel processor corresponding to an adjacent previous stage pixel, a token having segment information on a plane segment obtained when a polygon is cut by a scan line plane, said segment information including elements of a head pixel position (X), the number (dX) of successive pixels, the depth (Z) corresponding to the head pixel, a depth displacement (dZ/dX) for each pixel unit, the luminance data (I) corresponding to the head pixel, the luminance displacement (dI/dX) for each pixel unit, error data (EL) corresponding to the head pixel, and the error data (ER) corresponding to an end pixel;

means for outputting the token having the updated segment information to an adjacent subsequent pixel through one-stage pipe line register;

means for externally reading the data (Ib) in said luminance data; and

means for externally reading the error data in said error register;

wherein in the case where the plane segment information is input to said pixel processor, at a first timing T1, whether the pixel processor in question is included in the range where a new plane segment on the scan line in question is located is decided in the basis of the head pixel position (X) or the number (dX) of successive pixels input to said adder (12) by said inputting means, and if the pixel processor is within the range, at a second timing T2, the displacement data (dZ/dX) is added to the depth data (Z) by said adder to send its result to a subsequent pixel processor; at a third timing T3, the depth data (Z) is compared with the depth data in question in said depth register (10) by said adder (12) to decide whether Z < Zb or Z ≤ Zb, at a fourth timing T4, the change data (dI/dX) is added to the luminance data (I) by said adder (12) to send the result to a subsequent pixel processor, and only if the above decision result is yes, the contents of said depth register (10) and said luminance register (11) are replaced by the depth data (Z) and the luminance data (I) of the new plane segment; and at a fifth timing T5, whether the pixel processor in question is a head or end in the range on the scan where the new plane segment is located is decided on the basis of the head pixel position (X) or the number (dX) of successive pixels input to said adder (12), and only if the decision result is yes and also Z < Zb (or Z ≤ Zb), the contents of said error are replaced by the error data (EL) corresponding to the head pixel of the new plane segment and a symbol indicative of the head pixel or the error data (ER) corresponding to the end pixel and a symbol indicative of the end pixel according as the pixel processor in question is at a head or end in the range on the scan line

where the new plane segment is located; and wherein in the case where a sweep token indicative of the end of one scan line is input to a previous pixel processor in place of the token having the segment information, after the data (Ib) stored in said luminance register (11) and the data (EL) or (ER) in said error register (15) are externally output, the contents of said depth register (10) are initialized to a maximum value, those of said luminance register (11) are initialized to background color, and those of said error register (15) are initialized to an initial state, and said sweep token is outputted to a subsequent pixel processor.

4. An anti-aliasing method comprising the steps of error decision of, on the basis of errors of the coordinate values of two successive pixels on one scan line and error information deciding if the errors are due to a left boundary, a right boundary or the part other than the boundaries, deciding a combination of said items of error information and selecting errors of said two pixels; correction calculation of, on the basis of an input of said errors and pixel information of said two pixels, calculating an average (proportional distribution) of said pixel information between said two pixels in their area using said decision result; and replacement output of, on the basis of the said decision result, said correction calculation result and said pixel information, outputting said pixel information of said two pixels after it has been decided whether or not they should be replaced by the correction calculation result.

5. An anti-aliasing method comprising the steps of:
error decision of deciding, on the basis of inputs of errors En, En + 1, and items of error information Fn, Fn + 1, a combination of the items of error information Fn, Fn + 1 thereby to select En if the combination is that of a right boundary and the part other than boundaries or that of a right boundary and a right boundary, En + 1 if the combination is that of the part other than boundaries and a left boundary, or that of a left boundary and a left boundary, and a not smaller one of En and En + 1 if the combination is that of a right boundary and left boundary;
correction calculation of calculating, on the basis of inputs of the error En or En + 1 selected by the error decision device and luminance data In, In + 1 for successive pixels onone scan line, I = {(In + In + 1) + Ex (In - In + 1)}/2 (where x = n or n + 1); and
replacement output, on the basis of inputs of the decision by the error decision step, the calculation result I by the correction calculation and the luminance data In, In + 1, for outputting the luminance data In replaced by the calculation result I by the correction calculation device if the combination of Fn and Fn + 1 is that of a right boundary and the part other than boundaries, or that of a right boundary and a right boundary, the luminance data In + 1 replaced by I if the combination is that of the part other than boundaries and a left boundary, or that of a left boundary and a left boundary, both luminance data In and In + 1 replaced by I if the combination is that of a right boundary and a left boundary, and outputting the luminance data In and In + 1 without being replaced by I in other cases, where In and In + 1 (n: integer ≥ 0) are two successive pixels on one scan line, En and En + 1 are errors in the coordinates of the respective pixels, and Fn and Fn + 1 are their error related information deciding if the error is due to the left boundary, the right boundary or the part other the boundaries.

6. In a graphics display device for displaying a three-dimensional polyhedral object on a two-dimensional screen, a three-dimensional graphics processing apparatus comprising:
a hidden-surface processing device wherein information on a plane segment obtained when a polygon is cut by a scan line plane is inputted for each scan line, the information including elements of a head pixel position, the number of successive pixels, the depth corresponding to the head pixel, a depth displacement for each pixel unit, the luminance data corresponding to the head pixel, the luminance displacement for each pixel unit, the error data corresponding to the head pixel and the error data corresponding to an end pixel, and hidden-surface processing and smooth shading are executed to output the luminance data corresponding to the pixels on one scan line and the error data at the boundaries of the polygon;
a correction calculation device for deciding the combination of Fn, Fn + 1, on the basis of inputs of said errors En, En + 1, and said items of error information Fn, Fn + 1, thereby to select En if the combination is that of a right boundary and the part other than boundaries or that of a right boundary and a right boundary, En + 1 if the combination is that of the part other than boundaries and a left boundary, or that of a left boundary and a left boundary, and a not smaller one of En and En + 1 if the combination is that of a right boundary and left boundary; a correction calculation device for calculating, on the basis of inputs of the error En or En + 1 selected by the error decision device and luminance data In, In + 1 for successive pixels on one scan line, I = {(In + In + 1) + Ex (In - In + 1)}/2 (where x = n or n + 1) where the In and In + 1 (n: integer ≥ 0) are the luminance data of two successive pixels produced from said hidden-surface processing device; En and En + 1 are errors in the coordinates of the respective pixels, and Fn and Fn + 1 are their error related information; and
a replacement output device, on the basis of inputs of the decision by the error decision device, the

calculation result I by the correction calculation device and the luminance data In, In + 1, for outputting the luminance data In replaced by the calculation result I by the correction calculation device if the combination of Fn and Fn + 1 is that of a right boundary and the part other than boundaries, or that of a right boundary and a right boundary, the luminance data In + 1 replaced by I if the combination is that of the part other than boundaries and a left boundary, or that of a left boundary and a left boundary, both luminance data In and In + 1 replaced by I if the combination is that of a right boundary and a left boundary, and outputting the luminance data In and In + 1 without being replaced by I in other cases.

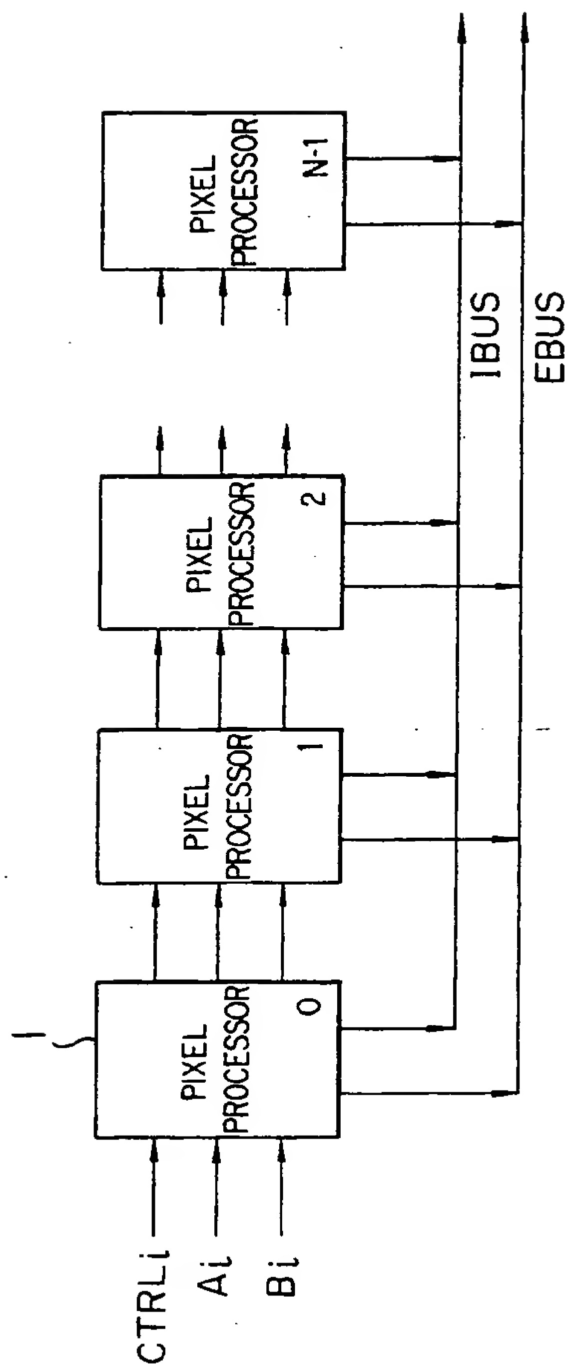
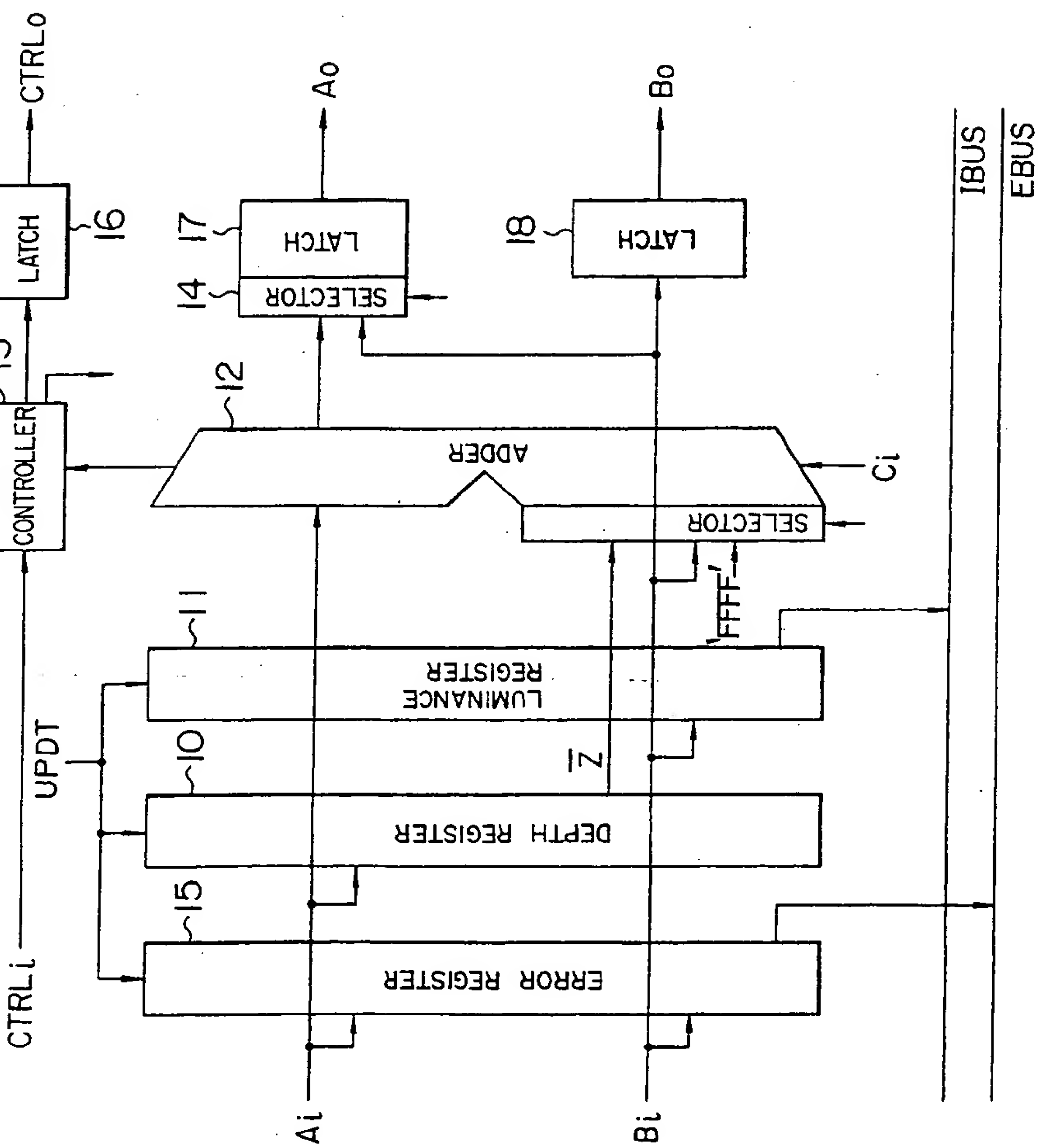

1
CTRLi
Ai
Bi
PIXEL PROCESSOR 0
PIXEL PROCESSOR 1
PIXEL PROCESSOR 2
PIXEL PROCESSOR N-1
IBUS
EBUS

FIG. 1


CTRLo
LATCH
16
Ao
17
LATCH
14
SELECTOR
Bo
18
LATCH
IBUS
EBUS
13
CONTROLLER
12
ADDER
Ci
SELECTOR
11
FFFF
LUMINANCE REGISTER
UPDT
10
Z
DEPTH REGISTER
15
ERROR REGISTER
CTRLi
Ai
Bi

F I G. 2

FIG. 3A

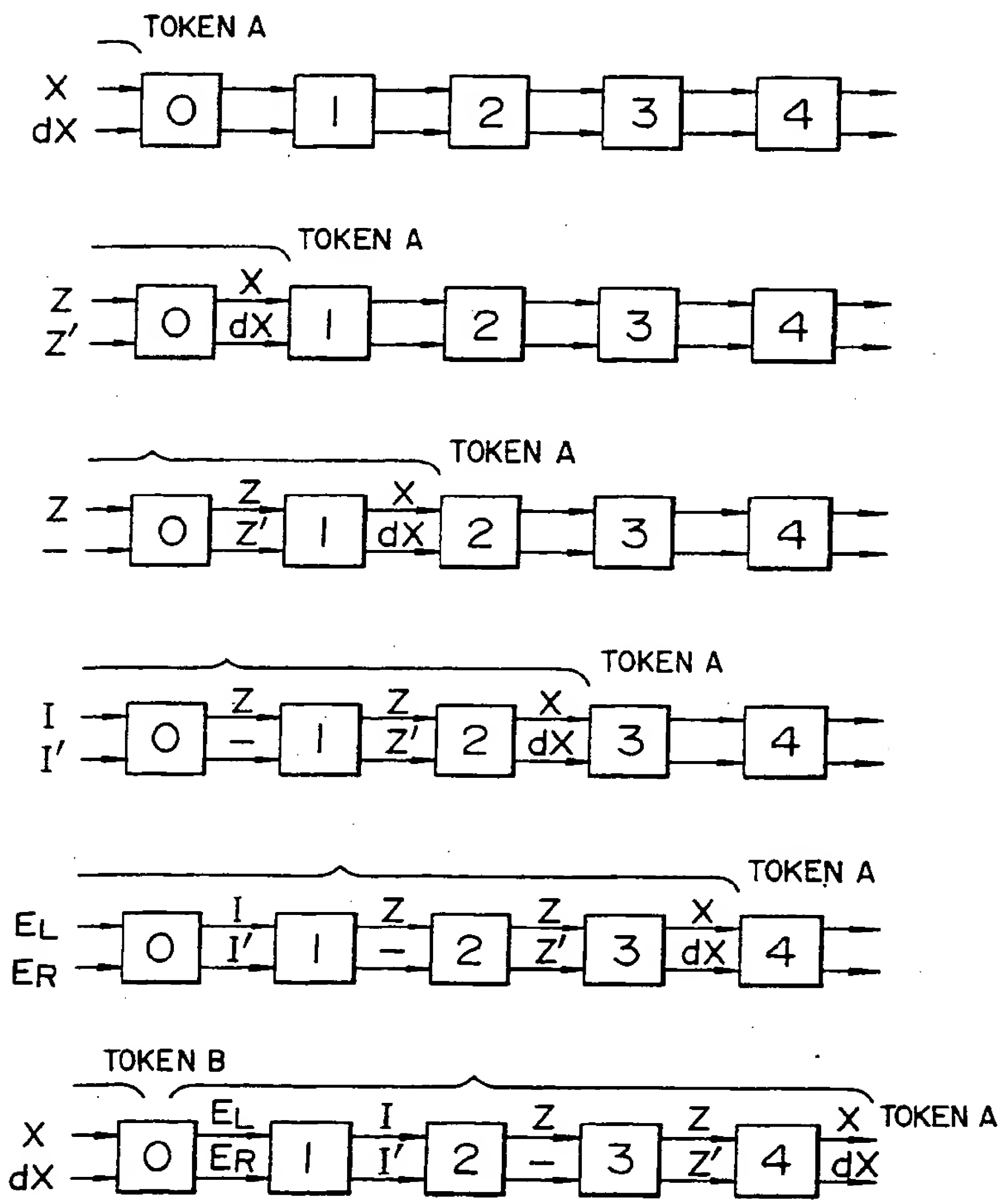
	CONTENTS
00	NOT BOUNDARY
01	RIGHT BOUNDARY
10	LEFT BOUNDARY

FIG. 3B

	CTRL	A PORT	B PORT
T_1	IN FLAG	X (IN = 0) dX (IN = 1)	dX
T_2	—	Z	Z'
T_3	—	Z	—
T_4	—	I	I'
T_5	—	E_L	E_R

FIG. 4A

FLOW OF SEGMENT TOKEN



F I G. 4B

FLOW OF SWEEP TOKEN

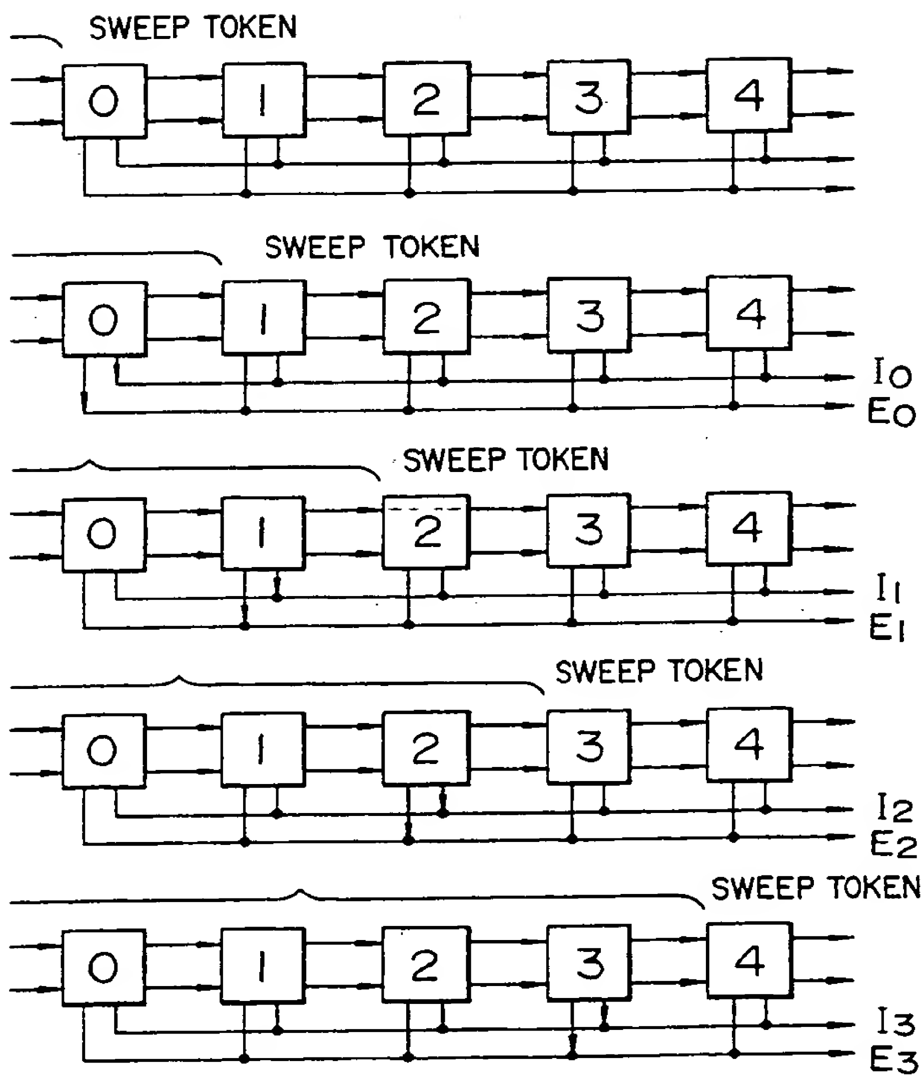


FIG. 5

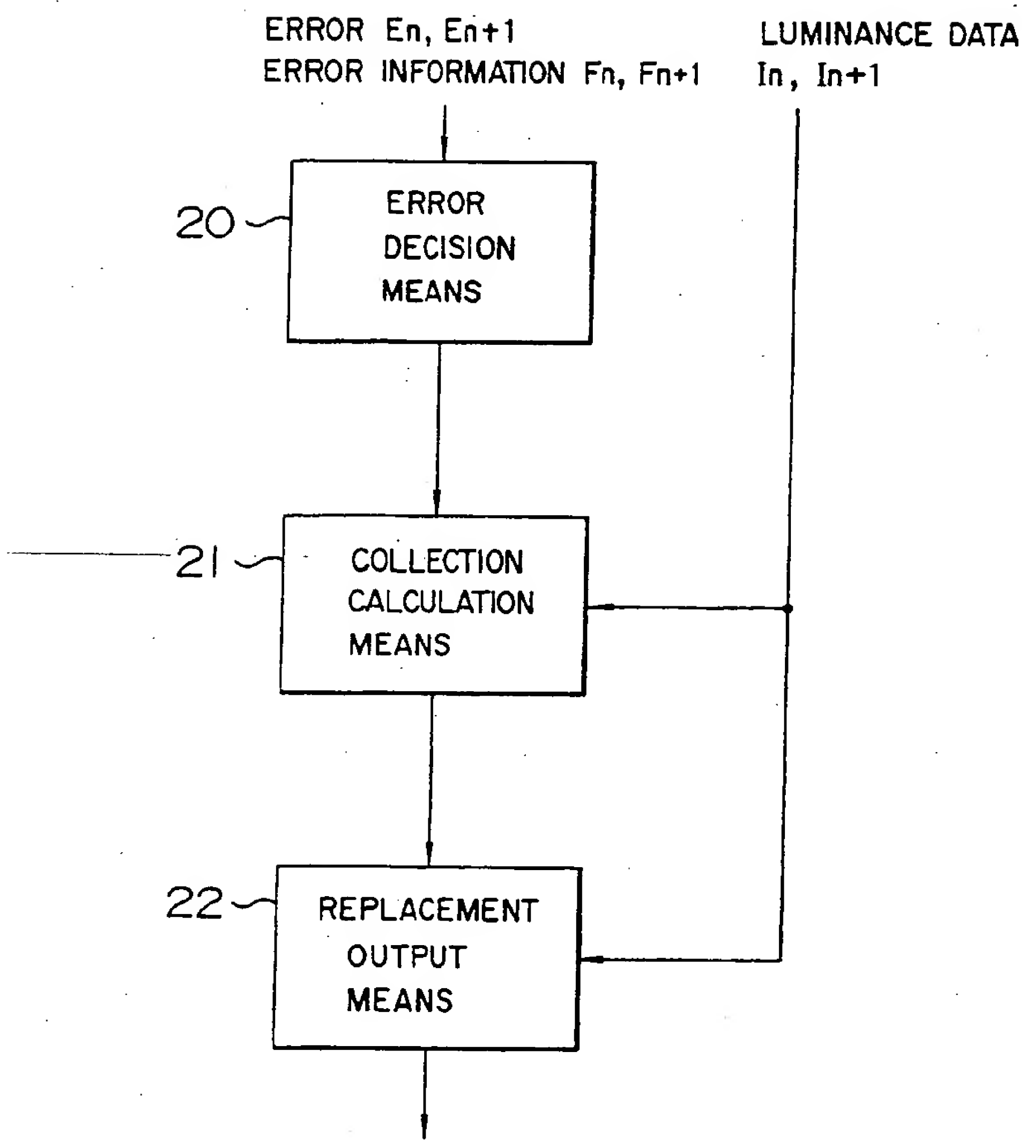

ERROR En, En+1
ERROR INFORMATION Fn, Fn+1
LUMINANCE DATA
In, In+1
20
ERROR
DECISION
MEANS
21
COLLECTION
CALCULATION
MEANS
22
REPLACEMENT
OUTPUT
MEANS

FIG. 6A

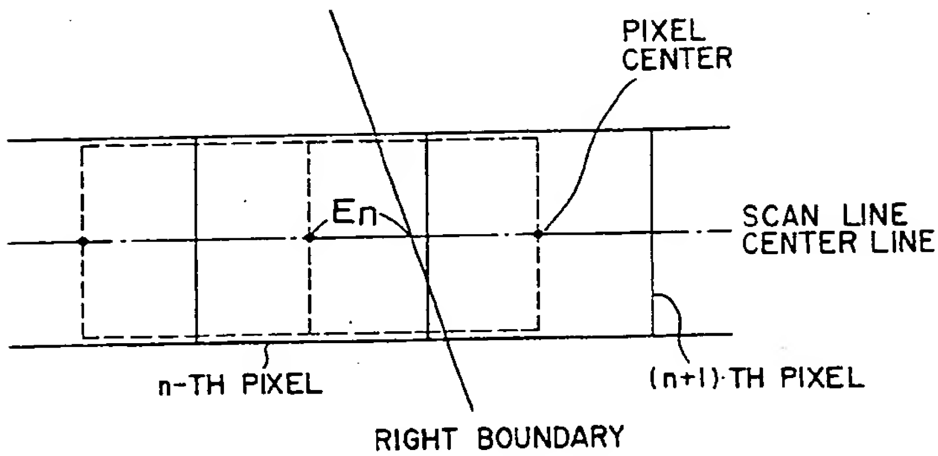
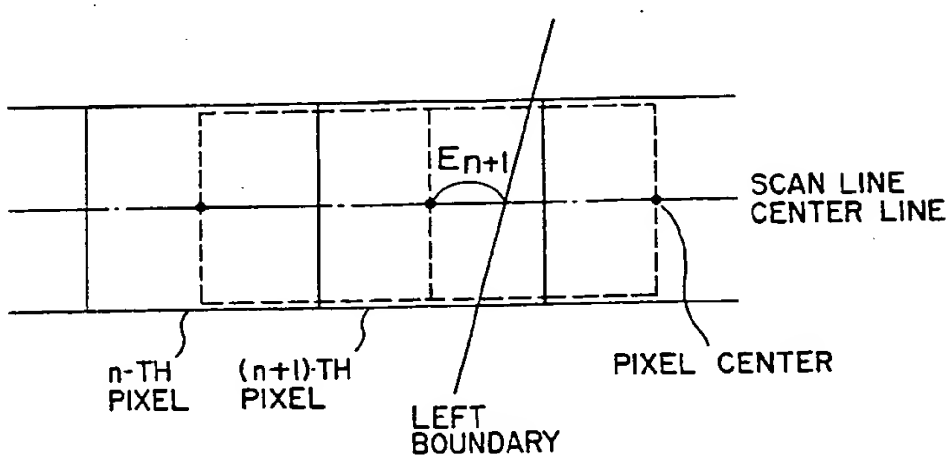

PIXEL
CENTER
En
SCAN LINE
CENTER LINE
n-TH PIXEL
(n+1)-TH PIXEL
RIGHT BOUNDARY

FIG. 6B


En+1
SCAN LINE
CENTER LINE
n-TH
PIXEL
(n+1)-TH
PIXEL
LEFT
BOUNDARY
PIXEL CENTER

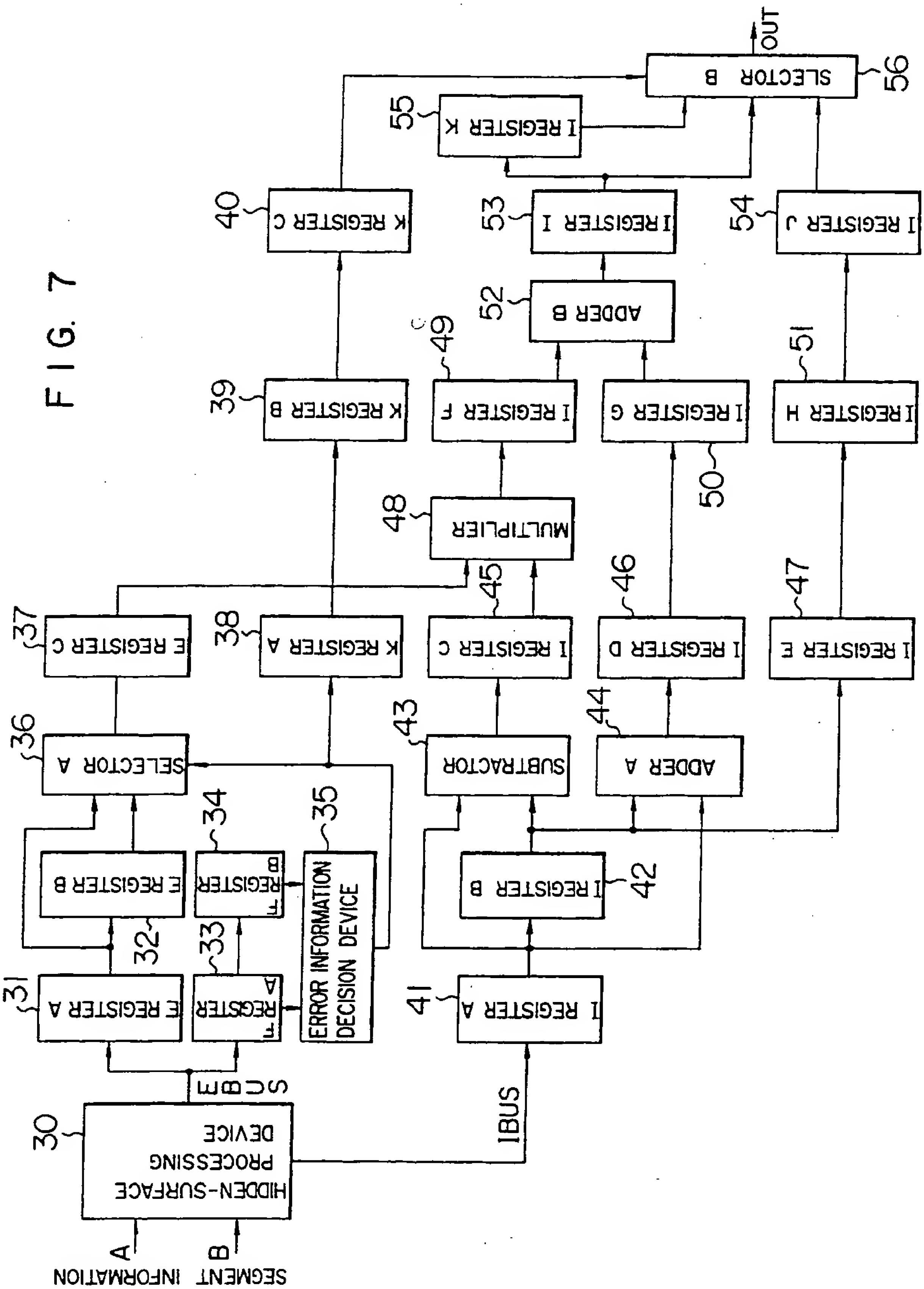

SEGMENT INFORMATION
A
B
HIDDEN-SURFACE PROCESSING DEVICE
30
EBUS
IBUS
E REGISTER A
31
32
F REGISTER A
33
E REGISTER B
F REGISTER B
34
ERROR INFORMATION DECISION DEVICE
35
SELECTOR A
36
E REGISTER C
37
K REGISTER A
38
K REGISTER B
39
K REGISTER C
40
I REGISTER A
41
I REGISTER B
42
SUBTRACTOR
43
ADDER A
44
I REGISTER C
45
I REGISTER D
46
I REGISTER E
47
MULTIPLIER
48
I REGISTER F
49
I REGISTER G
50
I REGISTER H
51
ADDER B
52
I REGISTER I
53
I REGISTER J
54
I REGISTER K
55
SLECTOR B
56
OUT

FIG. 7

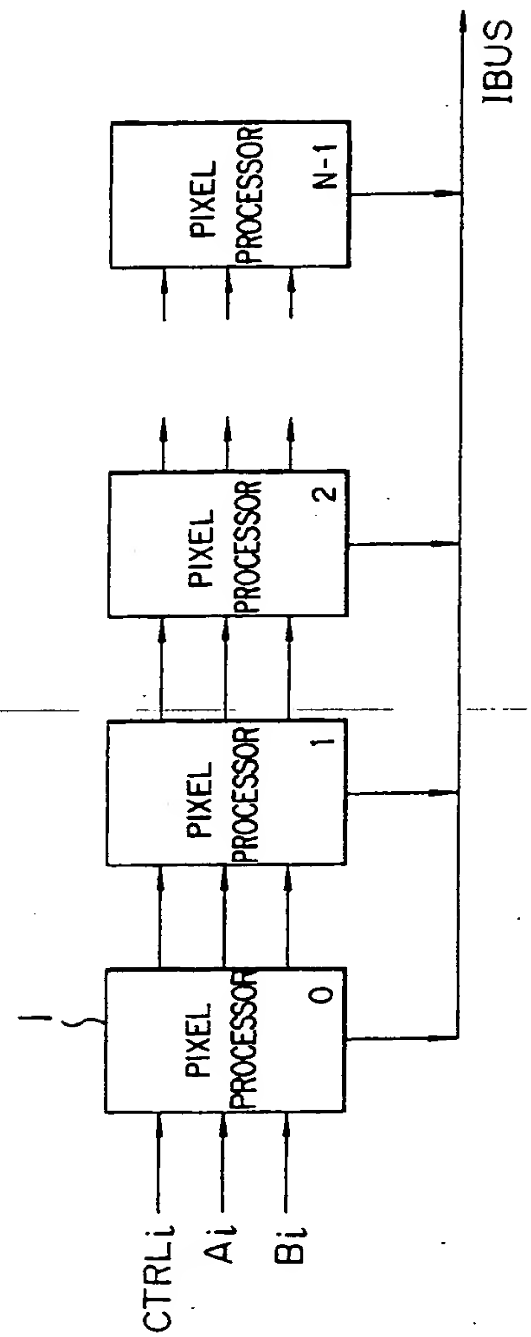
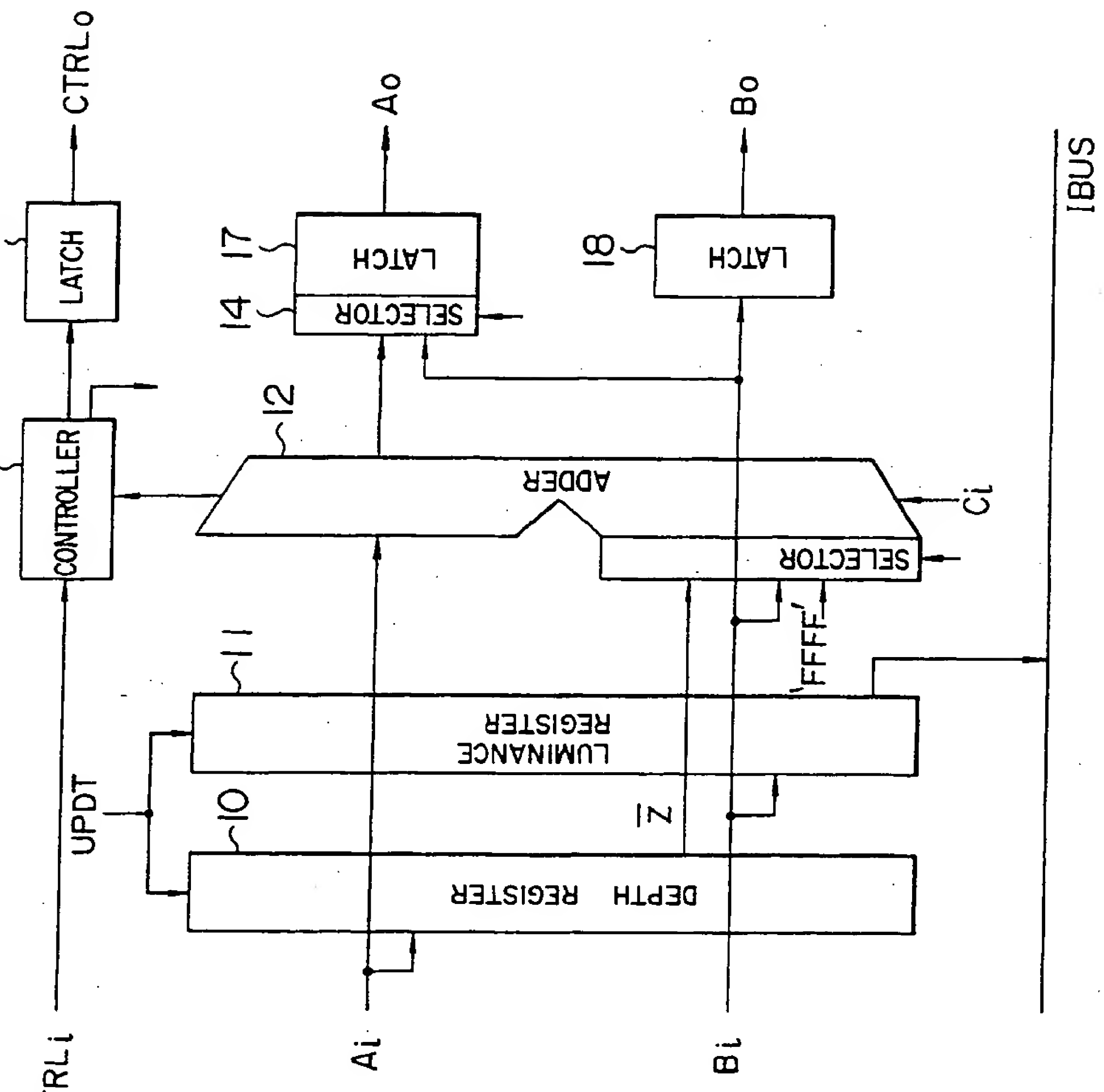

PIXEL PROCESSOR 0
PIXEL PROCESSOR 1
PIXEL PROCESSOR 2
PIXEL PROCESSOR N-1
CTRLi
Ai
Bi
IBUS

FIG. 8



CTRLi
Ai
Bi
CTRLo
Ao
Bo
IBUS
UPDT
Z
'FFFF'
Ci
DEPTH REGISTER
LUMINANCE REGISTER
ADDER
SELECTOR
CONTROLLER
LATCH
LATCH
LATCH
SELECTOR
10
11
12
13
14
16
17
18

FIG. 9

FIG. 10

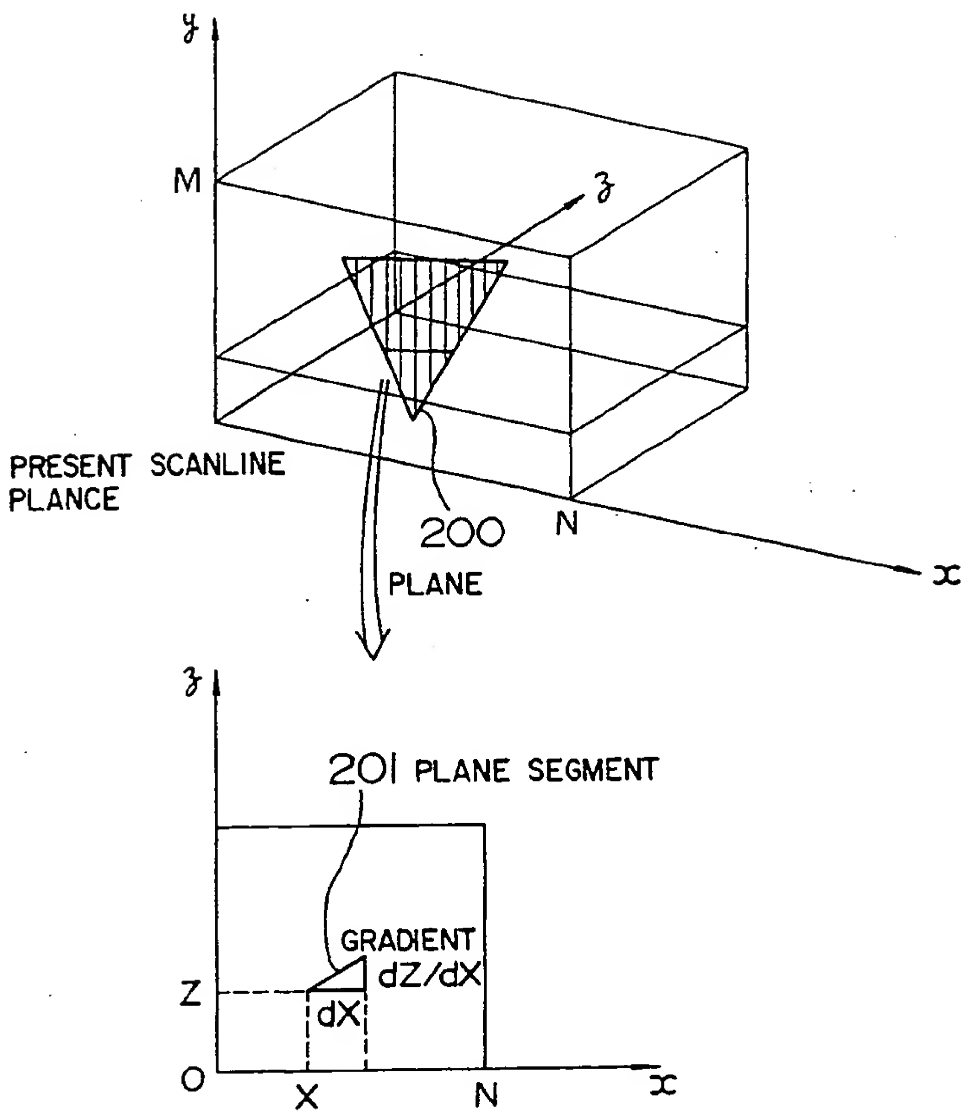

y
M
z
PRESENT SCANLINE
PLANCE
200
N
PLANE
x
z
201 PLANE SEGMENT
GRADIENT
dZ/dX
Z
dX
O
X
N
x

FIG. 11

	CTRL	A PORT	B PORT
T_1	IN FLAG	$\begin{cases} X & (IN = 0) \\ dX & (IN = 1) \end{cases}$	dX
T_2	—	Z	Z'
T_3	—	Z	—
T_4	—	I	I'

FIG. 12A

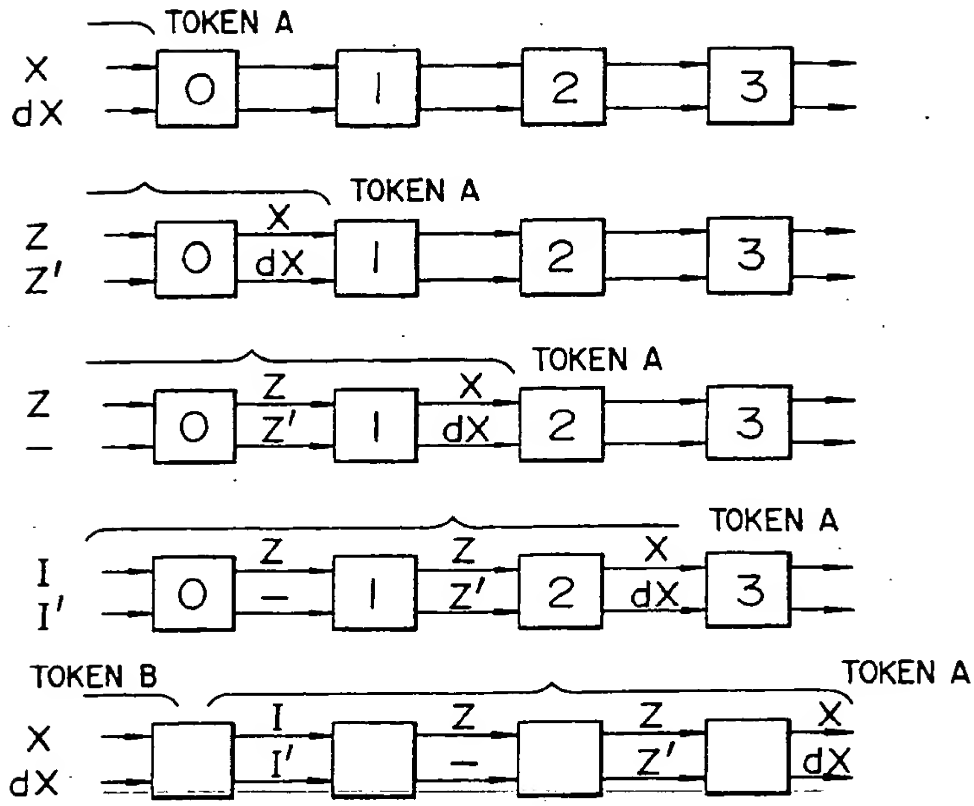


FIG. 12B

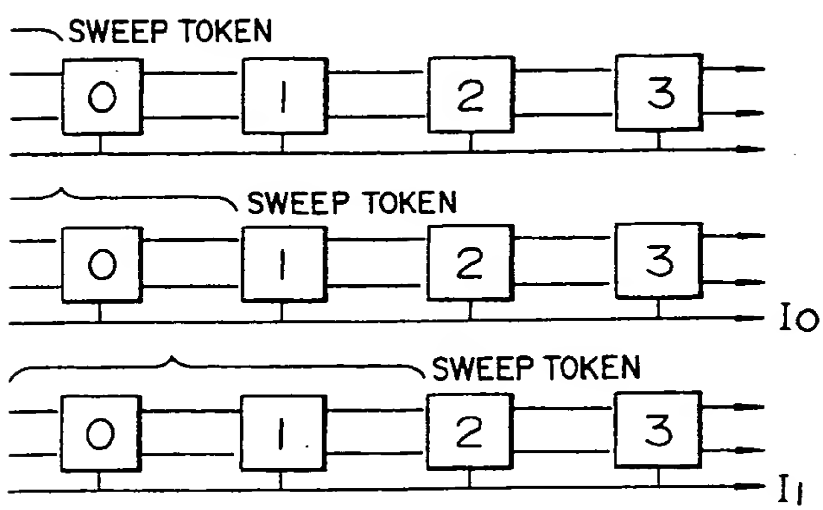


FIG. 13A

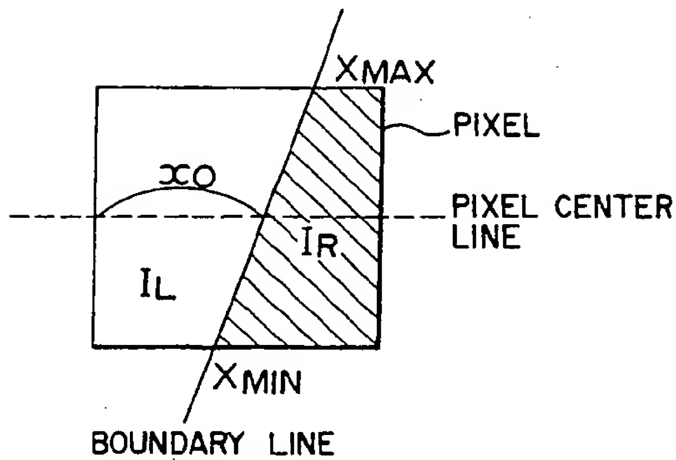


FIG. 13B

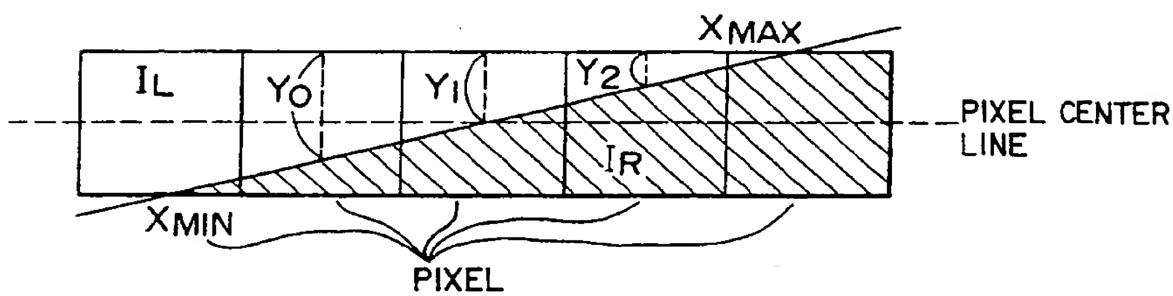
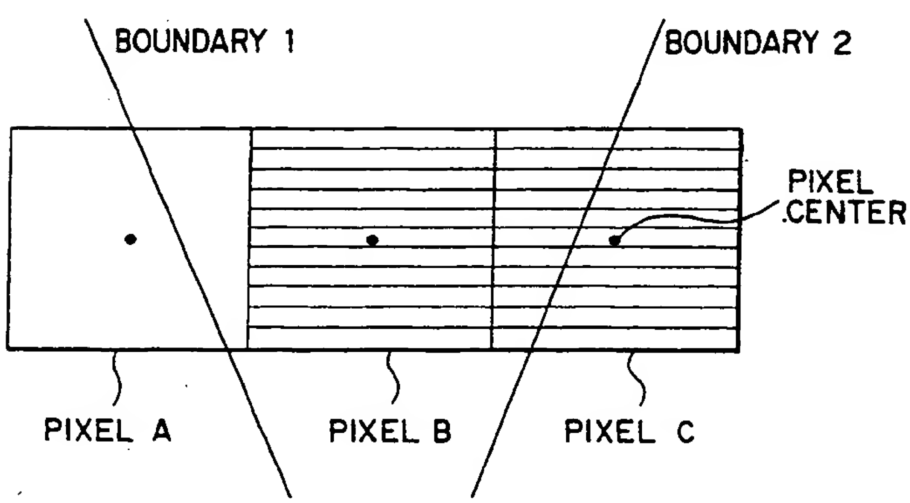


FIG. 14



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(54) Hidden-surface processing device, anti-aliasing method and three-dimensional graphics processing apparatus.

(57) The present invention intends to provide a three-dimensional graphics processing apparatus which can execute hidden-surface processing, smooth shading processing and anti-aliasing processing. The conventional hidden-surface processing device can only provide pixel information such as luminance data, and so cannot execute any processing requiring error data at polygon boundaries, such as anti-aliasing processing. The conventional anti-aliasing method must deal with many cases because the processing is made for each pixel, execute complicated calculation if the boundary line extends over several pixels, and may not able to process the display with decimals omitted. The hidden-surface processing device according to the present invention is provided with an error register (15) which can hold error data at polygon boundaries and its output means thereby to provide the error data at the polygon boundaries. The anti-aliasing method according to the present invention can replace the information on two successive pixels at polygon boundaries by its area average on two successive pixels on one scan line and output the replaced information, which is very efficient for real-time processing.

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EUROPEAN SEARCH REPORT

Application Number

EP 90 11 6294

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 5, October 1988, pages 1236-1240, New YorK, US; T. NISHIZAWA et al.: "A hidden surface and shading processor (HSSP) with a systolic architecture" * Whole document *	1-6	G 06 F 15/72
Y	US-A-4 371 872 (SINGER) * Whole document *	1-6	
A	COMPUTER GRAPHICS AND APPLICATIONS, vol. 4, no. 6, June 1984, pages 11-23, New York, US; A. FUJIMOTO et al.: "A 3-D graphics display system with depth buffer and pipeline processor" * Page 16, right-hand column, line 50 - page 21, left-hand column, line 3 *	1-6	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G 06 F 15/72

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	03 May 91	BURGAUD C.

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